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DEPLETION IMPLANT FOR POWER MOSFET

RELATED APPLICATION

[0001] This application claims the benefit of U.S. Provisional Application No. 60/271,550, filed February 26, 2001.

FIELD OF THE INVENTION

[0002] This invention relates to Power MOSFET devices and a process for their manufacture, and more specifically relates to a process and structure for preventing punch-through breakdown and reducing gate to drain charge (Q_{GD}) in low blocking voltage MOSFET devices.

BACKGROUND OF THE INVENTION

[0003] When a vertical conduction MOSFET is in a blocking mode, the inherent P/N body diode depletes toward the source. If there is insufficient charge in the channel (or body) region, punch-through occurs before avalanche breakdown is reached.

[0004] In a low voltage VDMOS device (Vertical Conduction Double Diffused MOS), this premature punch-through is normally prevented by using a higher channel dose and/or a deeper channel drive than might be otherwise required for a given avalanche breakdown value.

[0005] However, the higher channel dose results in a correspondingly higher threshold voltage V_{TH}; while a deeper channel drive increases channel length and thus channel resistance. The deeper channel drive also increases the depth of the JFET region between adjacent channel regions, thus reducing the optimum utilization of the epitaxial silicon receiving the diffusions.

oxide interlayer 27 is next deposited atop the wafer and is patterned to open windows to form contacts. The source regions are conventionally etched at their center to a given depth. An aluminum source contact 32 is then deposited atop the wafer and in contact with the N^+ type source regions 30 and the heavy base P^+ region 31.

[0017] In accordance with the invention, and prior to the field oxide step forming oxide 14 or prior to the gate oxide step forming gate oxide 15, a P type boron blanket implant of low concentration is applied over the top of the active surface of epi layer 13. This novel depletion implant will reduce the concentration in the channel region to help reduce the occurrence of punch-through, even though a low P concentration is used in the channel region (between channel and source perimeters) and will reduce the gate to drain charge of the final device. An N type depletion implant will be used for a P channel structure.

[0018] Figure 2 shows the doping concentration N as a function of depth in the die of Figure 1 from the silicon surface. Line 35 shows the concentration N_D of eptixial layer 13. Line 36 shows the P concentration (unadjusted) of the P channel regions 24. Line 37 shows the concentration of the N^+ sources 30. Line 40 shows the net P channel doping (in the invertible channels), which is the net P channel doping in regions 24, minus the N^- concentration 40.

[0019] The novel depletion implant, shown by line 42, of boron, (or some other P impurity) moves the net P concentration of the invertible channel 24 from line 40 to line 41, in accordance with the invention.

[0020] Clearly, if the invention is applied to a P channel device, an N depletion implant of arsenic or phosphorus is used.

[0021] Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other

uses will become apparent to those skilled in the art. It is preferred, therefore, that the present invention be limited not by the specific disclosure herein.

[0006] A process and structure which prevents punch-though without increasing channel dose or channel depth would be very desirable

BRIEF DESCRIPTION OF THE INVENTION

[0007] In accordance with the invention, a depletion implant is formed in the top surface of the epitaxial silicon for a low voltage (under 40 volts avalanche) MOSFET prior to the formation of the body and source diffusions. Thus, a boron blanket implant will be used in an N channel VDMOS (to reduce the net N type concentration); and an Arsenic or Phosphorus implant is used in a P channel VDMOS. The depletion implant enables the use of a lower channel implant dose and/or a shorter channel drive without getting into a punch-through condition before avalanche voltage is reached. This novel technique will also lower channel resistance which, for low voltage MOSFETs, (for example, 40 volts or less) is a significant portion of the device total on-resistance.

[0008] The depletion implant can be applied at any time prior to the channel diffusion, for example; before the first field oxidation; before gate oxidation or after the polysilicon etch but before the channel implant. Note that if the depletion implant is applied after the polysilicon etch that a deep drive thereof is required before the channel drive.

[0009] The novel depletion implant of the invention will put a uniform charge into the channel region, therefore preventing punch through as described above.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] Figure 1 is a cross-section of a small segment of an N channel DMOS die which receives the novel depletion implant of the invention.

[0011] Figure 2 shows the doping profile in Figure 1 near the epi surface and illustrates the presence and effect of the novel depletion implant.

DETAILED DESCRIPTION OF THE DRAWINGS

[0012] Figure 1 shows a small portion of an N channel VDMOS die 10 in cross-section. It should be noted that the invention also applies to P channel devices in which the concentration types are reversed from those shown in Figure 1.

[0013] The device comprises an N^+ substrate 11 having a bottom drain electrode metal 12 on its bottom. An epitaxially grown N^- layer ("epi") 13 is formed atop substrate 11 and is the junction-receiving layer of the device. The concentration N_D of N^- epi 13 is shown by the line 35 in Figure 2.

[0014] In the well known process for making the device of Figure 1, and delaying mention of the novel depletion implant of the invention, a field oxide is first formed on the upper surface of N^- epi 13. The field oxide is then removed in the active area of the device, leaving only the segment 14 shown in the termination region. Thereafter, a gate oxide 15 is grown atop the active area of die 10 and a conductive polysilicon gate layer 16 is grown above oxide 15. The polysilicon 16 and oxide 15 are then patterned to any desired stripe or cellular topology, and windows are opened therein. P type channel (or base) regions 24 are then implanted and diffused as shown. Boron may be conventionally used for this process.

[0015] The implant dose and diffusion drive time will determine the conductivity and depth of the channel regions 25. At the same time that windows are opened in layer 16, a conductive polysilicon field plate 26 (an extension of layer 16) is also defined in the termination region.

[0016] A source implant and drive are performed to form the source region 30. Then, a heavy base boron implant is done to form region 31 (P^+). An